Amendments to the Claims:

Please cancel withdrawn claims 1-6, and please add new claim 28 as follows. Please amend claims 7, 14-17, 19-23 and 26-27 as follows.

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. - 6. (canceled)

7. (currently amended) A method of manufacturing an SOI wafer, the method comprising:

a) forming an isolation insulating film on a front face of a first semiconductor wafer to define an active region and forming a bonding insulating film on a front face of a second semiconductor wafer;

b) forming a pad insulating film on the front face of the first semiconductor wafer;

[[b)]] c) after forming the pad insulating film, performing an ion implantation process so as to form a P-well and an N-well in the active region;

[[c)]] d) pre-bonding the respective front faces of the first semiconductor wafer including the active region having the P-well and the N-well, and the second semiconductor wafer;

[[d)]] e) heating the bonded first and second semiconductor wafers at a predetermined temperature to completely bond the first and second semiconductor wafers with each other; and

[[e)]] f) polishing a back face of the first semiconductor wafer to a bottom level of the isolation insulating film.

8. (original) The method of claim 7, wherein step a) comprises:

forming a mask insulating film on the surface of the first semiconductor wafer;

forming an isolation trench on the mask insulating film and the first semiconductor wafer;

forming a trench fill insulating film so as to bury the isolation trench; and

planarizing the trench fill insulating film to a level of the mask insulating film using a

planarization process.

9. (original) The method of claim 8, wherein the mask insulating film includes a silicon oxide film.

10. (original) The method of claim 9, wherein the mask insulating film further includes a silicon nitride film.

11. (original) The method of claim 8, wherein the trench fill insulating film is a silicon oxide film.

12. (original) The method of claim 8, wherein chemical mechanical polishing (CMP) is used in the planarization process.

13. (original) The method of claim 7, wherein in step a), the bonding insulating film is a silicon oxide film.

14. (currently amended) The method of claim 13, wherein the bonding insulating film is formed by thermally oxidizing ~~the substrate silicon of~~ the second semiconductor wafer.

15. (currently amended) The method of claim 7, wherein step [[b)]] c) comprises:

forming a photoresist having a pattern with which a region in which [[an]]the N-well is to be formed is opened, on the first semiconductor wafer;

implanting N-type impurities in ~~the substrate silicon of~~ the first semiconductor wafer using ion implantation and using the patterned photoresist as a mask; and

removing the photoresist.

16. (currently amended) The method of claim [[8]] 7, wherein step [[b)]] c) comprises:

forming a photoresist having a pattern with which a region in which [[a]]the P-well is to be formed is opened, on the first semiconductor wafer;

implanting P-type impurities in ~~the substrate silicon of~~ the first semiconductor wafer using ion implantation and using the patterned photoresist as a mask; and

removing the photoresist.

17. (currently amended) The method of claim [[16]]15, wherein the N-type impurities are 5-valence electron ions, including phosphorus (P), arsenic (As), and antimony (Sb).

18. (original) The method of claim 16, wherein the P-type impurities are 3-valence electron ions, including boron (B) and BF_2.

19. (currently amended) The method of claim 7, wherein step [[c)]] d) comprises:
arranging the first and second semiconductor wafers so that their respective front faces are adjacent each other; and

vertically applying a force to a back face of a bonded surface of the first and second semiconductor wafers.

20. (currently amended) The method of claim 19, wherein step [[c)]] d) further comprises absorbing certain H_2O vapor into the surfaces at which the first and second semiconductor wafers are bonded with each other.

21. (currently amended) The method of claim 7, wherein step [[d)]] e) is performed at a temperature higher than a temperature at which ions implanted in the N-well and the P-well form a well.

22. (currently amended) The method of claim 7, wherein step [[e)]] f) comprises:
preparing a back face of the first semiconductor wafer to be a polishing face; and

polishing ~~substrate silicon on~~ the back face of the first semiconductor wafer using a polishing process.

23. (currently amended) The method of claim 22, wherein polishing ~~the substrate silicon~~ comprises grinding the back face of the first semiconductor wafer using a grinder.

24. (original) The method of claim 22, wherein chemical mechanical polishing (CMP) is used as the polishing process.

25. (original) The method of claim 24, wherein in the polishing process, the isolation insulating film is used as a polishing stopper.

26. (currently amended) The method of claim 7, after step [[e)]] f), further comprising forming a sacrificial oxide film ~~protection insulating film~~ on the polished back face of the first semiconductor wafer. ~~a top surface of a semiconductor substrate.~~

27. (currently amended) The method of claim 26, wherein the ~~protection insulating~~ sacrificial oxide film is a silicon oxide film.

28. (new) The method of claim 26, further comprising:

removing the sacrificial oxide film using a wet etch process; and

forming a silicon insulating film using thermal oxidation and CVD on the polished back face of the first semiconductor wafer, thereby forming a protection insulating film on the back face.